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Nanotechnology Investigation of Ultra-shallow Junctions of Antimony (Sb) Implants in Conventional Silicon (Si)

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Abstract

The sheet resistance of the doped region in ultra-shallow junctions is critical to the speed of non-strained engineered integrated circuits. Maintaining low sheet resistance for antimony Sb implanted in Si is a difficult challenge to meet the performance requirements of future Complementary Metal Oxide Semiconductor devices (CMOS). A developed Differential Hall Measurements (DHM) is utilized to measure the dopant carrier concentration profile matches with the atomic profile measured by Secondary Ion Mass Spectroscopy (SIMS) for electrical characterization of the formed ultra-shallow junction. Present results show that decreasing the ion implant energy as 40 keV, 12 keV, 5 keV and 2 keV for the given implant dose under rapid thermal annealing (RTA) in the range from 600°C to 1100°C for 10s, results in an increase in sheet resistance from ~200 Ω/sq to ~850 Ω/sq with reduction in electrical activation percentage from ~90% to ~30%. Also the conductivity mobility decreases with implant energy while increases with annealing temperature. This reduction in electrical activation is due to reduction in junction depth from 60 nm at 40 keV to 17 nm at 2 keV accompanied with higher peak Sb concentration ($\geq 2 \times 10^{20}$ cm^{-3}) as implant energy decreases for annealing temperature less than 800°C for 10s. Higher annealing temperature (i.e. > 800°C) does not improve the electrical activation while increases the sheet resistance due to the out diffusion of Sb from the active region. The best results that nearly satisfying industrial ITRS requirements corresponds to the following parameters: 5 keV implant energy with sheet resistance 400 Ω/sq, electrical activation 60%, conductivity mobility 50 cm^2/Vs, peak Sb concentration of 4×10^{20} cm^{-3} and junction depth 22 nm.

Keywords: Antimony doped Si; Ion implantation; Differential hall effect; Rapid thermal annealing; Shallow junction formation

Introduction

Antimony "Sb" is resisting deactivation more than arsenic "As", since it has heavier mass with lower diffusivity when implanted in non-strained and strained silicon "Si". So Sb seems to be a potential alternative and more stable as a common n-type spices used for ultra-shallow doping of engineering CMOS devices. Sheet resistance of CMOS devices is critical to the speed of integrated circuits. Therefore, heavily doped ultra-shallow junctions are required to achieve low resistance in Source/Drain region [1-4]. The Source/Drain junction depth χ$_j$ which has traditionally been controlled by ion implantation is one of the challenged critical dimensions that need to be scaled (nano-scaled) and engineered for modern CMOS [5]. Varying the dopant implant energy and dopant dose with low thermal budget processing becomes one of the important approaches to generate ultra-shallow junctions. For low thermal budget, there are three techniques: flash annealing, laser annealing and rapid thermal annealing. RTA has the advantage which give rise to solid phase epitaxial regrowth (SPER) of the radiation damaged region due to ion implantation. RTA induced SPER has demonstrated the highest dopant solubility for As and Sb as well as maximizing the activation of dopants [6,7]. The electrical characterization of the implanted junction layer is well profiled by matching the carrier concentration profile results from Differential Hall effect measurements (DHM) with atomic profile investigated by Secondary Ion Mass Spectroscopy (SIMS). Alzanki et al. [8] investigated the effect of ion implant dose (1×10^{14} cm^{-2} - 1×10^{15} cm^{-2}) for low implant energies (2 keV and 5 keV) on the atomic profiles, carrier profiles and sheet resistance. The results show that the optimum electrical characteristics of the formed shallow junction and its sheet resistance require much lower thermal budget than the currently used in industry. Also Bennett [9,10] investigated the effect of implant dose (1×10^{14} cm^{-2} - 1×10^{15} cm^{-2}) for 2 keV implant energy for controlled Si and strained-engineered Si. The results indicate that the strained Si enhances the carrier mobility by ~30% which reduces the sheet resistance by ~30% for junction depth of ~10 nm to 15 nm. Combination of Rutherford Back Scattering (RBS) results with Medium Energy Ion Scattering (MEIS) results [11] could determine the lattice site occupancy of Sb implanted in conventional Si and strained Si for 2 keV and 40 keV. These results were compared with that measured by DHM and prove that the Hall Scattering factor "r", which appeared in the following equations, is equal to unity is valid even the peak concentration peaks at $\geq 2 \times 10^{20}$ cm^{-3}. It is known that this scattering factor is a correction factor due to effects of circulating currents resulting from varying of carrier

scattering degrees caused by the presence of the magnetic field in Hall measurements. The correlation between sheet resistances (R_s), sheet Hall coefficient R_{HS}, and the scattering factor could be described by:

$$R_s = \frac{1}{\chi_j \sigma_s} = \frac{1}{e \int_0^x N_s(\chi) \, \mu_c d\chi} \qquad (1)$$

$$R_{Hs} = \frac{r}{eN_s} \qquad (2)$$

and

$$\mu_c = \frac{R_{Hs}}{rR_S} \qquad (3)$$

Where χ_j is the junction depth of the implanted layer, Ns is the sheet carrier density, is the electron charge and μ_c is the conductivity mobility. Differential Hall effect Measurements (DHM) coupled with X-ray Photoelectron Spectroscopy (XPS), were applied by Su et al. [12] to investigate the deactivation of phosphorous laser annealed ultra-shallow junction. The results indicate a carrier profile redistribution near surface due to uphill diffusion caused by phosphorous deactivation. Dong et al. [13] provide a novel shallow doping technique with low temperature processing, investigated by Auger electron spectroscopy and Hall effect measurements, provides great potential in fabrication of high efficiency silicon Nanowire (SiNW) solar cell. This technique proves formation of a shallow junction with phosphorous surface concentration above 1×10^{20} cm^{-3} and junction depth 10 nm. This shallow junction enhances the short circuit current of radial SiNW by 7.75% compared to the axial PN junction solar cell. High current with low-energy (400 eV) ion implantation and low-energy temperature microwave annealing is employed by Tsai et al. [14] to achieve ultra-shallow junction. They used two-step microwave annealing which is more effective. In the first step annealing, a high power (2400 W; ~500°C) was utilized to achieve Solid Phase Epitaxial Regrowth (SPER) and enhance microwave absorption. In the second step of annealing, unlike in conventional thermal annealing, which requires higher energy to activate the dopant, a 600 W (250°C) microwave is used to achieve low sheet resistance. The device subjected to this two-step annealing (2400 W for 300 s + 600 W for 600s) has the lowest threshold voltage Vth and lowest Sub-threshold Swing (SS), so highest cap ability to control the sub-threshold current. Liang et al. [15] studied the effect of annealing on the properties of boron implanted emitter for n- silicon solar cell by comparing Rapid Thermal Annealing (RTA) and Furnace Annealing (FA) conditions. They simultaneously employed Hall effect measurements and RBS techniques to probe into the effects of annealing on the electrical properties of boron implanted samples. They concluded that the cell received annealing at 1000°C for 20 min exhibited the lowest dark saturation current density J_o, the lowest damaged spectra, the highest free carrier density (N_s) and the highest efficiency 18.85%, whereas those receiving lower thermal budgets exhibited lower performance due to the increased recombination accompanied with RTA. In this work, an investigation is carried out to determine the optimum electrical parameters of the antimony implanted layer for p-type Si that match the industrial requirements. The effect of rapid thermal annealing RTA on the optimum values of sheet resistance R_s, electrical activation E_a%, conductivity mobility μ_c, sheet carrier density N_s, peak carrier concentration and junction depth χ_j are examined for different implant energies (40 keV, 12 keV, 5 keV and 2 keV) as well as at different annealing temperatures (from 600°C to 1100°C for 10s). An implant dose of 4×10^{14} cm^{-2} is adapted in all investigated implant energies as it provides the lowest sheet resistances among all the studied cases.

Experimental Details

P-type (100) Si wafers of diameter 100 nm with resistivity of 10-12 Ω cm were implanted at room temperature with antimony ions of implanted energies 2 keV, 5 keV, 12 keV and 40 keV for doses in the range from 1×10^{14} cm to 1×10^{15} cm. Here we treated the energies data with doses 4×10^{14} cm^{-2}, 5×10^{14} cm^{-2}, 8.5×10^{14} cm^{-2} and 4×10^{14} cm^{-2}, respectively. The doses around 4×10^{14} cm^{-2} gave the best results for the formed shallow junctions. The tilt and twisted angles in the implantation were 7° and 22°, respectively. The wafer were cut into small pieces and activated using a process product corporation RTP system in the temperature range from 600°C to 1100°C for times between 5 seconds and 3600 seconds in flowing nitrogen gas. However the majority of samples were annealed for 10 s as longer annealing times produced insignificant difference in electrical activity or sheet resistance. Wide set of measurements with an accent HL5500 Hall system. Several samples were measured for each experimental point and the average is taken. The estimated uncertainty in sheet resistance values is in the range 2.5-4%. Details of the technique could be found in Alzanki et al. [11] and Bennett et al. [10]. The differential Hall Technique is a complicated method for characterizing ultra-shallow doping in semiconductors but with careful experimental protocol and considered data analyses it can merit reliable results, since it has a unique advantage over other techniques as it capable of separating the relative carrier concentration and mobility distribution to the conduction of the doped layer under test. Also samples were analyzed as-implanted and annealed using SIMS technique for atomic concentration profiles by CAMECA IMS 6F with primary beam energy of 750 eV O$_2^+$ for 5 keV to 40 keV for Sb whilst for 2 keV Sb a 500 eV Cs$^+$ beam was used for analyses to ensure reliable profile shape and dose in the near surface region.

Results and Discussion

Atomic profiles and carrier profiles

Figure 1 shows the atomic profiles simulated by the TRIM2003 software for implant energies 2 keV, 5 keV, 12 keV and 40 keV and atomic profiles determined from SIMS measurements of 2 keV and 5 keV. As shown from these profiles the projected range estimated from TRIM simulation increases from 5 nm to 26 nm as implant energy increases from 2 keV to 40 keV while there is a decrease of peak atomic concentration of as implanted samples from 3.5×10^{21} cm^{-3} to 3.8×10^{20} cm^{-3}, respectively. Also, SIMS atomic profiles are shallower and more broaden at tails than the simulated TRIM profiles with lower peak concentration.

This difference may be attributed to the fact that Sb suffers from radiation enhanced diffusion during implantation.

Figure 2 shows SIMS atomic profile after rapid thermal annealing at 600°C and 800°C for 10 s at implant energies 2 keV and 5 keV. The important note here is that the peak concentration and the peak depth of 5 keV are similar to as-implanted (shown previously in Figure 1) and the annealed values 9×10^{20} cm^{-3} at 5.3 nm and 8.5×10^{20} cm^{-3} at 5.5 nm are within the accepted experimental error. Also for 2 keV the atomic profiles are similar for as-implanted and the annealed one (1.7×10^{21} cm^{-3}) but the peak depth is shallower after annealing as it changes from 4.5 nm to 3.3 nm.

Figure 3 presents a comparison between two SIMS atomic profiles with the corresponding two carrier concentration profiles for 5 keV implant energy with doses varying from 5×10^{14} cm^{-2} to 1×10^{15} cm^{-2} after annealing at 800°C. In this figure, the carrier concentration profiles are identical considering accepted experimental error. It is clear from the figure that it is only measure part of the carrier distribution because of the close proximity of the n$^+$/p junction and the high resistance associated with the resulting depletion region. This means that there is no advantage in implanting a dose above 5×10^{14} cm^{-2}.

Electrical characterization of the implanted layer

For rapid thermal annealing ≤ 800°C: In this Section we discuss the electrical parameters extracted from the SMIS atomic profiles and DHM carrier profiles for samples annealed at RTA from 600°C and 800°C for 10s at different implant energies. Figures 4 and 5 show the variation of sheet resistance R$_s$ (Ω/sq) and the electrical activation percentage (E$_a$%) with annealing temperature for different implant ion energy. As seen from Figure 4, as the implant energy decreases from 40 keV to 2 keV at annealing temperature of 700°C for 10s, the sheet resistance proves significant increase from 200 Ω/sq to 850 Ω/sq respectively. In the same time, Figure 5 indicates decrease in electrical activation from 90% to 30% when the implant energy decreases from 40 keV to 2 keV at 700°C for 10s. The increase in sheet resistance illustrated in Figure 4 as well as the
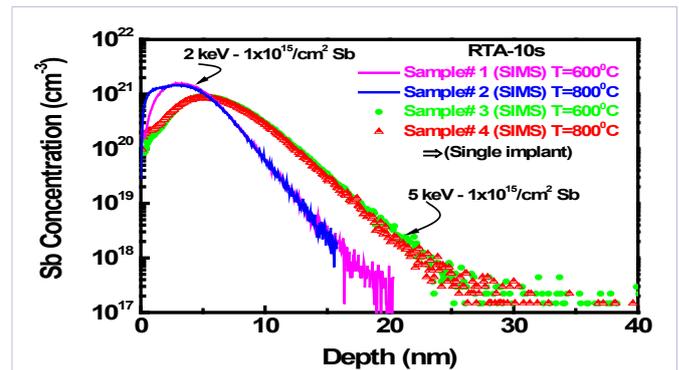

Figure 2: SIMS atomic profile after rapid thermal annealing at 600°C and 800°C for 10s at implants energies 2 keV and 5 keV.
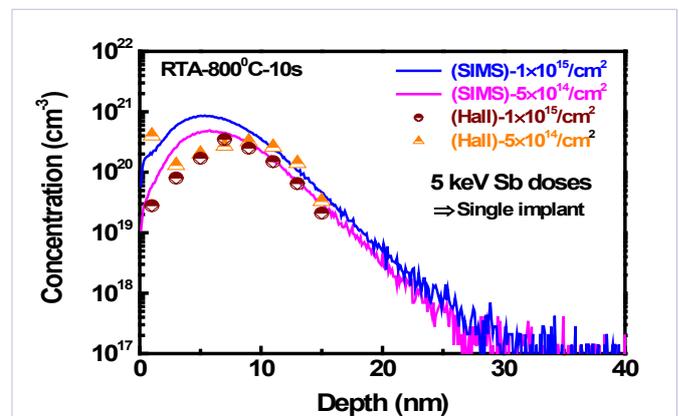

Figure 3: Comparison between SIMS atomic profiles and corresponding carrier concentration profiles for 5 keV implant energy.

decrease in electrical activation illustrated in Figure 5 can be mainly attributed to the decrease in the thickness of the formed junction with decreasing the implanted energy and to also the decrease in sheet carrier density Ns as indicated in equations (1-3). This behavior is accompanied with increase and shallower of the peak carrier concentration as will be discussed in the following sections. In addition, sheet resistance presented in Figure 4 exhibits an exponential increase with the increase of the annealing temperature from 600°C to 1100°C. This exponential increase is faster as the implant energy decreases from 40 keV to 2 keV. Also, Figure 5 shows a decrease in electrical activation with the increase of the annealing temperature which is faster at annealing temperature 900°C. This may be related to the low thermal budget caused by RTA process. Where RTA process give rise to the Solid Phase Epitaxial Regrowth (SPER) which allows the structure to return to a more stable crystalline form and can maximize the activation of the dopant Sb, but SPER is related to the dopant solubility level. This solubility level is lowered by increase of the annealing temperature which causes reduction in Sb activation as shown in Figure 5 and increase of sheet resistance shown in Figure 4. This increase of sheet resistance and the decrease of electrical activation with the increase of the annealing temperature from 600°C to 800°C in conventional Si is discussed in details by Horan et al. [6] and Bennett et al.
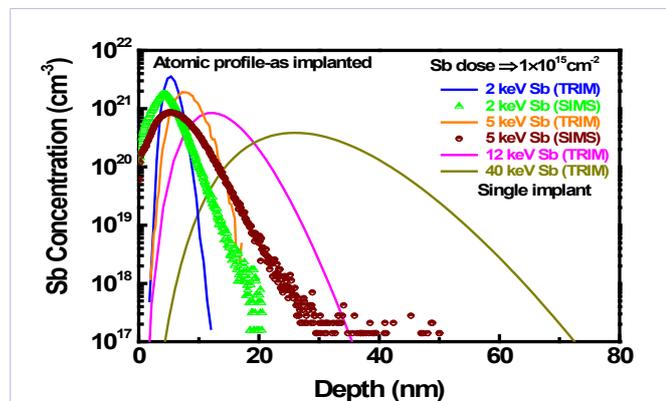

Figure 1: Comparison between atomic profiles simulated by TRIM2003 software and corresponding atomic profiles determined from SIMS measurements for different implant energies.
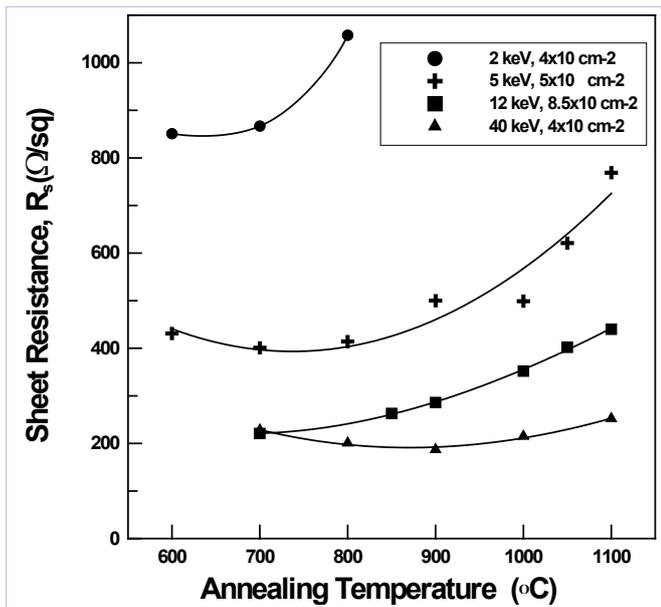
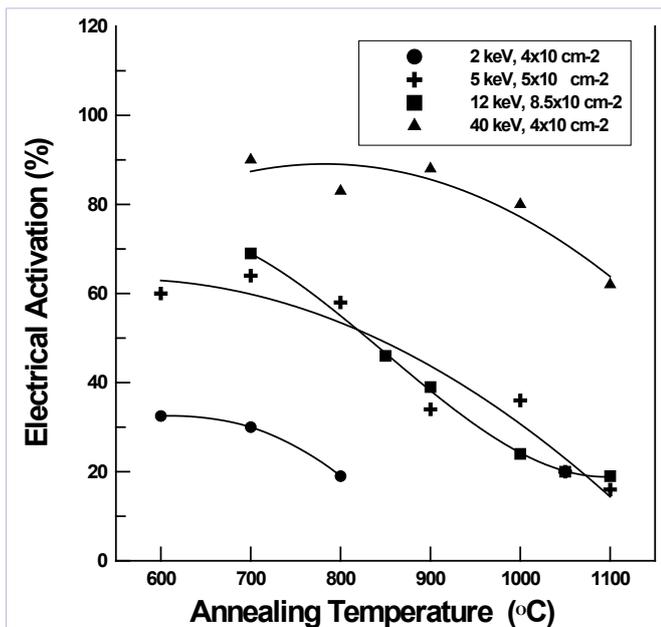**Figure 4:** Variation of sheet resistance with annealing temperature.

Figure 5: Variation of electrical activation with annealing temperature.

[10]. They suggested that the reduction in Sb activation is not a consequence of Sb deactivation at elevated temperature but is a result of different regrowth rate due to solubility level.

For rapid thermal annealing > 800°C: For high temperature annealing > 800°C, there is a significant broadening of the electrical profiles, so the electrical activation decreases rapidly. This is because Sb atoms tend to cluster and/or precipitate together at higher temperatures and this is unavailable for electrical activation. During rapid thermal annealing two mechanisms compete: the first is the regrowth of the damaged layer with inclusion of the dopant atoms in the lattice sites

available for electrical conduction (as explained SPER), while the second is the diffusion of the dopant that tends to nucleate to form inactive precipitates. Increasing thermal energy higher than 800°C, the second mechanism starts to dominate the first one.

Carrier mobility

Mobility is one of the important parameters used to characterize electrically the implanted layer. The mobility values depend on the annealing temperature, the implant energy and the implant dose as shown in Figure 6. In this figure the mobility values are lowest at 600°C, where with increasing the annealing temperature the defects removed and the crystallinity of the lattice improves, so the mobility improves. This mobility behavior with the increase of the implant energy can be discussed with the results of the sheet carrier density N_s in Figure 7 and the peak concentration obtained from SIMS and DHM profiles presented in Figure 8. The results in Figure 8 shows a decrease of sheet carrier density N_s by decreasing the implant energy (except some data of 12 keV which will be discussed later) and this in turn causes the decrease of the mobility as the implant energy increases from 2 keV to 5 keV to12 keV. Whereas for implant energy 40 keV the variation of the mobility curve with annealing temperature has higher values than all other data since 40 keV has more implant depth compared to the other lower energies, so the dopant is more deeper and maybe there is a net reduction in vacancy concentration in the near surface region. This is illustrated in Figure 8 where 40 keV peak concentration data are the lowest one which is proved by combining the measurements of Rutherford Back scattering RBS with Medium Energy ion Scattering MEIS measurements for 40 keV samples (Alzanki et al. [11]). It is observed that there is overlap of results for electrical activation curve (Figure 5) and mobility curve (Figure 6) at 5 keV and 12 keV, which can be attributed to the results of sheet carrier density Ns (Figure 7) where the values of 12 keV samples have Ns greater than other samples for ≤ 900°C, which may reduce the electrical activation presented in Figure 5 and overlap with mobility of 5 keV (Figure 6). This increase of Ns for 12 keV may be due to its higher implant dose (at 8.5×10^{14} cm^{-2}) which lead to higher probability precipitation which decreases the Sb activation and increases the mobility values so that it overlap with the results of 5 keV. Figure 8 presents the data of peak carrier concentration with annealing temperature at different implant energies. As the implant energy decreases, the junction depth decreases and so the peak concentration increases from 2×10^{20} cm^{-3} for 40 keV to 3×10^{20} cm^{-3} for 5 keV and increases to 1.5×10^{21} cm^{-3} for 2 keV. This increase of peak concentration reflects the reduction in sheet carrier density Ns with the decrease of implant energy and this leads to improvement in mobility. Also the peak carrier concentration decreases by increasing the annealing temperature which reduces the defect and improves the regrowth, so as a result the mobility improved for all implant energies.

Junction depth

The technology roadmap semiconductors identify three requirements for ultra-shallow junctions:
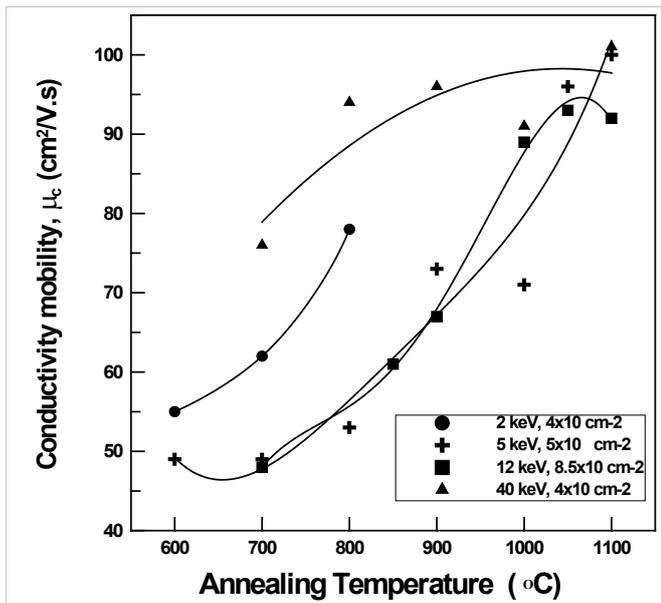
(i)Reducing the junction depth which could be achieved by

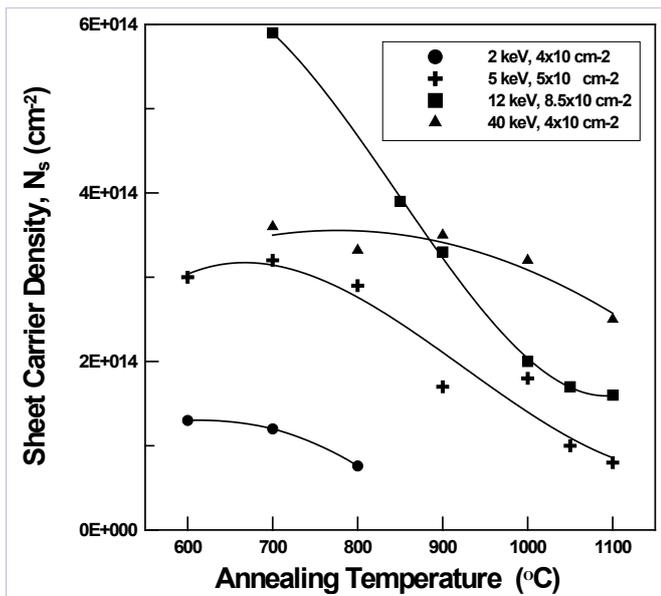**Figure 6:** Variation of carrier mobility with annealing temperature.

Figure 7: Variation of sheet carrier density with annealing temperature.

lowering the implant energy with varying the implant dose.

(ii)Increasing the junction steepness which could be achieved mainly by exchanging the type of the substrate of conventional Si to strained-engineered Si and trying other dopants [6,9] which enhances the conductivity mobility and the junction steepness.

(iii)Maintaining lower sheet resistance, recent studies (Horan et al. [6] & Alzanki et al. [8]) have shown that Sb is a potential competitive of as to be as n-COMS Source/Drain extension dopant choice for his point.

The first two requirements (i) and (ii) are more easily to be achieved, while the third junction concerning lowering the sheet

resistance is a difficult challenge specially for conventional Si, since sheet resistance is inversely related to the carrier mobility, the dopant electrical activation and the junction depth as indicated from Equation (1).

Figure 9 presents the variation of sheet resistance R_s of present measured samples as function of the shallow and ultra-shallow junction depth along the one of the industry requirements of the roadmap technology. The results of 2keV implant energy produce an ultra-shallow junction ~17 nm with lowest sheet resistance ~850 Ω/sq which is still higher than that of roadmap. However,
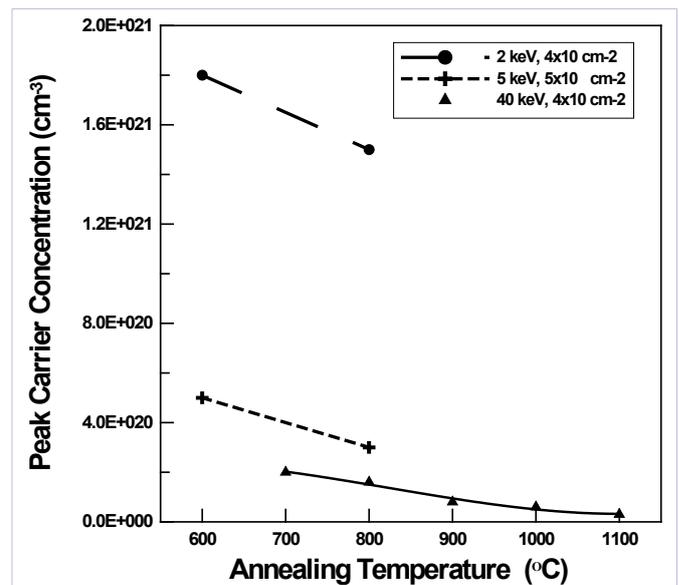

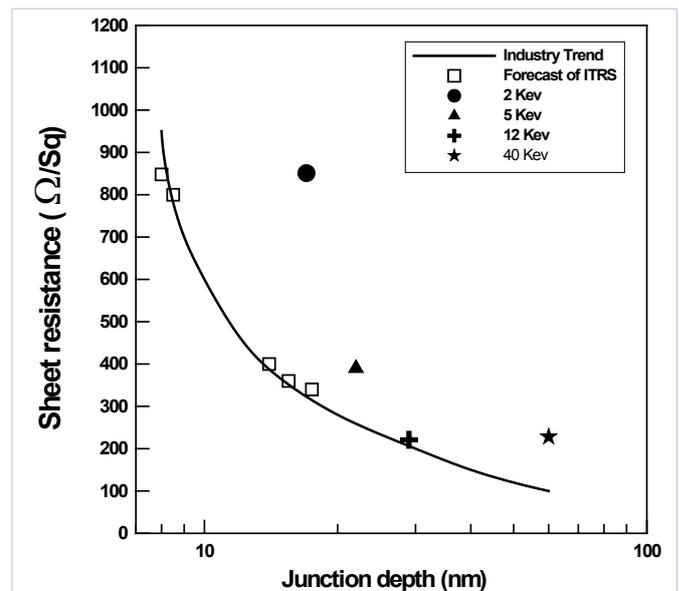**Figure 8:** Variation of peak carrier concentration with annealing temperature.

Figure 9: Variation of sheet resistance R_s of present measured samples as function of the shallow and ultra-shallow junction depth along the one of the industry requirements of the roadmap technology.

one can state that results of low implant energy of 5 keV matches well with that of roadmap technology at junction depth ~22 nm with sheet resistance 400 Ω/sq, electrical activation 60%, conductivity mobility 50 cm^2, sheet carrier density ~3 × 10^{14} cm^{-2}, and peak concentration 5 × 10^{20} cm^{-3}, which proves that the concentration of implanted antimony exceeds its solubility limit in comparison with arsenic as reported by Suzuki et al. [16].

Conclusions

Antimony implantation in silicon seems a promising candidate to achieve ultra-shallow, heavy doped and low resisting source/drain extensions. Differential Hall effect measurements in conjunction with new layer removal technique has been developed and matched with SIMS measurements to obtain reproducible carrier and mobility shallow doping profiles of Sb implanted in Si with nanometer resolution. The main effects of the two important parameters: implant energy and low thermal annealing budget are:

For RTA ≤ 800°C

•Low thermal budget by RTA process results in negligible diffusion and shallow junctions of Sb implantation in Si, while As implantation in Si requires high thermal budget (RTA > 900°C)

•A decrease of implant energy from 40 keV to 2 keV results in:

1-A decrease in electrical activation from ~90% to ~30%.

2-An increase of sheet resistance from ~200 Ω/sq to ~850 Ω/sq.

3-An increase of peak carrier concentration from ~2 × 10^{20} cm to values > 5 × 10^{20} cm^{-3}.

4-Shallower of the junction depth from ~60 nm to ~17 nm.

•When the low thermal budget is employed the junction depth does not increase during SPER, this important finding makes Sb an interesting alternative dopant species for modern CMOS.

•Best results are that of 5 keV which nearly matches well the ITRS requirements with electrical activation 60%, Sheet resistance 400 Ω/sq and junction depth 22 nm.

For RTA > 800°C

All implant energies diffusion of antimony is recoded with significant broadening of the electrical profiles which rules out the use of high temperature processing.

Acknowledgements

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Page 6 of 6